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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/421,322	10/18/1999	HIROYUKI OI	PM-264817/OS	3971

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EXAMINER

ECKERT II, GEORGE C

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 12/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/421,322

Applicant(s)
Oi et al.

Examiner
George C. Eckert II

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Jul 2, 2002
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 3, 5, 6, and 9 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 3, 5, 6, and 9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other: _____

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DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated May 28, 2002 in which claims 1, 3 and 5 were amended has been entered of record.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by EP 0 493 116 to Ohta et al (from IDS, Paper #12). Ohta et al. teach, with reference to figures 1a to 1o, a dielectrically separated wafer 13 having a plurality of dielectrically separated monocrystalline

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silicon islands (note the islands are formed from silicon layer 1 which is a doped monocrystalline silicon layer, col. 4, line 3), mutually defined by a dielectrically separating oxide film 6 on the surface of the wafer, wherein the dielectrically separated islands 12 comprise:

a high concentration impurity layer 2 (col. 4, line 6) formed on the bottom of the islands in a flat plate form; and

a low concentration impurity layer 12 having an identical conductivity (n-, col. 4, line 3) laminated on the plate of the high concentration layer.

With regard to claim 5, Ohta et al. teach, with reference to figures 1n and 1o, a dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands, separated by a dielectrically separating oxide film 6 on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat (see figures 1n and 1o which shows that the separated wafer has a surface between the distinct island), by controlling the polishing (grinding) of the silicon and dielectric layer (col. 7, lines 20-31).

3. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by JP 02-52452 to Katayama et al. (from IDS, Paper #12). Katayama et al. teach, with reference to figures 2a-2i, a dielectrically separated wafer (generally 2') having a polysilicon layer 14 and a plurality of monocrystalline silicon islands 2d mutually separated by a dielectrically separating layer 12

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consisting of silicon oxide (see *Constitution*) which is formed on a surface of a polysilicon layer 14, wherein:

the polysilicon layer is formed from a seed layer 20 formed by a low temperature CVD method (note page 270, upper right hand side of Katayama et al. where it is taught that layer 20 is formed by a CVD process at 650°C) on an interface with the dielectrically separating oxide film (see fig. 2g) and a polysilicon layer 14 formed by a high temperature CVD method (note page 270, lower left hand side, of Katayama et al. where it is taught that layer 14 is formed at 1150 - 1230°C). Note the instant specification, page 16, lines 5-7 which teaches a low temperature CVD process has a temperature of 550 - 700° C and a high temperature CVD process has a temperature of 1200 - 1300° C.

4. Claim 6 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ohta et al. Ohta et al. taught the device of claim 5 above but did not expressly disclose that a flatness on the surface of the dielectrically separated islands is less than 0.2 μm when measured by a stylus-profilometer. However, this limitation is considered either taught by Ohta et al. or, in the alternative, obvious over the same. That is, Ohta et al. teach that the oxide and silicon are ground (col. 7, lines 20-31) to form the islands. As such, it is considered inherent that the grinding will create a surface having no difference between the maximum and minimum values of flatness. In the alternative, it is considered obvious that the surface of the device of Ohta et al. would be formed to have a flatness as instantly claimed.

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Though Ohta et al. do not expressly disclose any value of a surface roughness, it is considered within the skill of a mechanic in the art to minimize any surface roughness as motivated by the relationship, known in the art, between surface roughness and complications of processing subsequent layers (alignment issues, planarity issues affecting wiring parameters, etc.). Therefore, claim 6 is considered either inherent or obvious over that taught by Ohta et al.

5. Claim 9 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Katayama et al. Katayama et al. taught the device of claim 3 above but did not expressly disclose that a flatness on the surface of the dielectrically separated islands is less than 0.2 μm when measured by a stylus-profilometer. However, this limitation is considered either taught by Katayama et al. or, in the alternative, obvious over the same. That is, Katayama et al. teach that both surfaces 2a and 2b are polished flatwise (*Constitution*) to form the islands. As such, it is considered inherent that the polishing will create a surface having no difference between the maximum and minimum values of flatness. In the alternative, it is considered obvious that the surface of the device of Katayama et al. would be formed to have a flatness as instantly claimed. Though Katayama et al. do not expressly disclose any value of a surface roughness, it is considered within the skill of a mechanic in the art to minimize any surface roughness as motivated by the relationship, known in the art, between surface roughness and complications of processing subsequent layers (alignment issues, planarity issues affecting wiring

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parameters, etc.). Therefore, claim 9 is considered either inherent in, or obvious over that taught by Katayama et al.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 3, 5, 6, and 9 have been considered but are moot in view of the new grounds of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GECKERT
GEORGE ECKERT
PRIMARY EXAMINER

GCE
December 6, 2002